



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER OF PATENTS AND TRADEMARKS Washington, D.C. 20231 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/877,027	06/11/2001	Yasuhiko Tsukikawa	57454-138	9823
75	590 01/25/2002			
McDERMOTT, WILL & EMERY			EXAMINER	
600 13th Street Washington, Do	, N.W. C 20005-3096		NGUYEN, LINH M	
			ART UNIT	PAPER NUMBER
			2816	
			DATE MAILED: 01/25/2002	

Please find below and/or attached an Office communication concerning this application or proceeding.

			\sim			
	Application	No.	Applicant(s)			
Office Action Comme	09/877,027		TSUKIKAWA, YASUHIKO			
Office Action Summary	Examiner		Art Unit			
	Linh M. Ngu		2816			
The MAILING DATE of this communication Period for Reply	ation appears on the c	over sheet with the o	correspondence address			
A SHORTENED STATUTORY PERIOD FOR THE MAILING DATE OF THIS COMMUNIC. - Extensions of time may be available under the provisions of after SIX (6) MONTHS from the mailing date of this commun. - If the period for reply specified above is less than thirty (30) or if NO period for reply is specified above, the maximum stature. - Failure to reply within the set or extended period for reply with any reply received by the Office later than three months after earned patent term adjustment. See 37 CFR 1.704(b). Status	ATION. 37 CFR 1.136(a). In no event, lication. days, a reply within the statutor tory period will apply and will express the application.	however, may a reply be tir y minimum of thirty (30) day pire SIX (6) MONTHS from	nely filed s will be considered timely. the mailing date of this communication.			
1) Responsive to communication(s) filed	d on <u>11 June 2001</u> .					
2a)☐ This action is FINAL . 2b)⊠ This action is no	n-final.				
3) Since this application is in condition for closed in accordance with the practice	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposition of Claims						
4)⊠ Claim(s) <u>1-17</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5)⊠ Claim(s) <u>11-13</u> is/are allowed.						
6)⊠ Claim(s) <u>1,4 and 14</u> is/are rejected.						
7)⊠ Claim(s) <u>2,3,5-10 and 15-17</u> is/are objected to.						
8) Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9)☐ The specification is objected to by the Examiner.						
10)⊠ The drawing(s) filed on <u>11 June 2001</u> is/are: a)⊠ accepted or b)⊡ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
11)☐ The proposed drawing correction filed on is: a)☐ approved b)☐ disapproved by the Examiner.						
If approved, corrected drawings are required in reply to this Office action.						
12)☐ The oath or declaration is objected to by the Examiner.						
Priority under 35 U.S.C. §§ 119 and 120						
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).						
a)⊠ All b)□ Some * c)□ None of:						
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
14) ☐ Acknowledgment is made of a claim for o	domestic priority unde	⁻ 35 U.S.C. § 119(e) (to a provisional application).			
a) The translation of the foreign langu 15) Acknowledgment is made of a claim for a Attachment(s)	- ,					
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-3) Information Disclosure Statement(s) (PTO-1449) Paper		Notice of Informal P	(PTO-413) Paper No(s) atent Application (PTO-152)			
S. Patent and Trademark Office TO-326 (Rev. 04-01)	Office Action Summary		Part of Paper No. 4			

Application/Control Number: 09/877,027

Art Unit: 2816

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ooishi (U.S. Patent No. 6,324,118).

With respect to claim 1, 4, and 14, Fig. 15 of Ooishi discloses a semiconductor device comprising a delay locked loop and corresponding method including: a) an input buffer [231] for receiving an external clock [CLK] and outputting a first internal clock [ECLK]; a delay circuit [238] for delaying the first internal clock to output a second internal clock [ECLK2]; a detector [232] for detecting a phase difference between said first and second internal clocks, and a counter [234], being responsive to an output of the detector for generating a signal adjusting an amount of delay of the delay circuit. Ooishi does not disclose a gray code counter using a gray code, being responsive to an output of said detector. Barrett, Jr. et al. discloses, in col. 4, lines 35-44, the use of a gray code counter and its advantage. To configure Ooishi's delay locked loop with Barrett Jr. et al.'s gray code counter in lieu of Ooishi's counter would have been obvious

Application/Control Number: 09/877,027

Art Unit: 2816

to one of ordinary skills in the art at the time of the invention since such a configuration has been well-known in the art for the requirement of minimal power consumption as evidenced by the teachings of Barrett Jr. et al. (see col. 4, lines 35-44).

Allowable Subject Matter

Claims 11-13 are allowed.

Claims 2-3, 5-10, and 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Prior art of record does not show or fairly suggest 1) a gray code counter including a) a gray code register storing said gray code; b) a binary code converter converting said gray code into a binary code; c) an upward carry/downward carry generator using said binary code stored in said binary code converter, to generate an upward carry signal and a downward carry signal; and d) a carry multiplexer generating from said upward carry signal and said downward carry signal a carry signal corresponding to a result obtained by said detector, for updating said gray code in said gray code register, as called for in claims 2, 5, and the corresponding method claim 15, and 2) a delay locked loop including a combination of a) a first input buffer receiving at least a first external clock and a second external clock complementary in phase to the first external clock, and outputting a first internal clock at the timing of the rising edge of the first external clock when a potential of the first external clock is equal to that of the second external clocks, and outputting a second input buffer receiving at least said first and second external clocks, and outputting a second internal clock at the timing of the rising edge of

Page 4

the second external clock when a potential of the first external clock is equal to that of the second external clock; c) a first delay circuit delaying the first internal clock to output a third internal clock; d) a second delay circuit delaying said second internal clock to output a fourth internal clock; e) a detector detecting a phase difference between the first and third internal clocks; and f) a gray code counter using a gray code, responsive to an output of the detector for generating a signal adjusting an amount of delay of the first delay circuit and an amount of delay of the second delay circuit, as called for in claim 11.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (703) 305-0414. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:30 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703) 308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-0142 for regular communications and for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Link M. nguyer